IN THE CLAIMS:

Please cancel claims 37 and 38, amend claims 19 and 24, and add new claims 48-52. All other claims are included for the convenience of the Examiner.

1. (Previously Presented) A method, comprising:

executing an instruction that updates data in a register at a first time;

storing an instruction address of the instruction;

when the data is not read from the register at a next clock cycle from completion of execution of the instruction, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address of the instruction is encountered a second time and the bit indicates that the instruction is a slowable instruction, delaying processing of the instruction.

2 – 4. (Previously Cancelled)

5. (Previously Presented) The method of claim 1, wherein when the instruction address of the instruction is encountered the second time, the bit is examined to determine if the instruction is a slowable instruction.

6. (Previously Presented) The method of claim 1, wherein delaying the processing of the instruction comprises delaying decoding the instruction.

7. (Previously Presented) The method of claim 1, wherein delaying the processing of the instruction comprises using lower priority resources to execute the instruction.

8. (Previously Presented) The method of claim 1, wherein delaying the processing of the instruction comprises delaying loading the data into the register until prior to the data is read from the register.

9. (Previously Presented) A method, comprising:

recording a first clock cycle when an instruction that loads data into a register is to complete;

storing an instruction address of the instruction;

recording a second clock cycle when the data is read from the register;

when the second clock cycle is more than one clock cycle from the first clock cycle, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address is encountered a next time, and the bit indicates that the instruction is the slowable instruction, delaying processing of the instruction.

10 – 14. (Previously Cancelled)

15. (Previously Presented) The method of claim 9, wherein the processing of the instruction is delayed by delaying decoding the instruction.

16. (Previously Presented) The method of claim 9, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

17. (Original) The method of claim 9, wherein information about the first clock cycle and the second clock cycle is provided by a scheduler.

18. (Original) The method of claim 17, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.

19. (Currently Amended) A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:
executing an instruction that loads data into a register at a first time; [and]
storing an instruction address of the instruction;
when the data is not read from the register at a next clock cycle from completion of execution of the instruction, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and
when the instruction address of the instruction is encountered a second time and the bit indicates that the instruction is a slowable instruction, delaying processing of the instruction.

20 - 23. (Previously Cancelled)

24. (Currently Amended) The computer readable medium of claim 19, [bwherein] wherein delaying the processing of the instruction comprises delaying decoding the instruction.

25. (Previously Presented) The computer readable medium of claim 19, wherein delaying the processing of the instruction comprises using lower priority resources to execute the instruction.

26. (Previously Presented) The computer readable medium of claim 19, wherein delaying the processing of the instruction comprises delaying loading the data into the register until prior to the data is read from the register.

27. (Previously Presented) A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:

recording a first clock cycle when an instruction is to complete storing data in a register;

storing an instruction address of the instruction;

recording a second clock cycle when the data is read from the register;

when the second clock cycle is more than one clock cycle from the first clock cycle, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address is encountered a next time, and the bit indicates that the instruction is the slowable instruction, delaying processing of the instruction.

28 - 32. (Previously Cancelled)

33. (Previously Presented) The computer readable medium of claim 27, wherein the processing of the instruction is delayed by delaying decoding the instruction.

34. (Previously Presented) The computer readable medium of claim 27, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

35. (Original) The computer readable medium of claim 27, wherein information about the first clock cycle and the second clock cycle are provided by a scheduler.

36. (Original) The computer readable medium of claim 35, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.

37. (Cancelled)

38. (Cancelled)

48. (New) A system, comprising:

a memory; and

a processor coupled to the memory and to perform operations comprising:

executing an instruction that updates data in a register at a first time;

storing an instruction address of the instruction;

when the data is not read from the register at a next clock cycle from completion of execution of the instruction, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address of the instruction is encountered a second time and the bit indicates that the instruction is a slowable instruction, delaying processing of the instruction.

49. (New) The system of claim 48, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

50. (New) The system of claim 48, wherein the processing of the instruction is delayed by delaying decoding the instruction.

51. (New) A system, comprising:

means for recording a first clock cycle when an instruction that loads data into a register is to complete;

means for storing an instruction address of the instruction;

means for recording a second clock cycle when the data is read from the register;

when the second clock cycle is more than one clock cycle from the first clock cycle, means for setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address is encountered a next time, and the bit indicates that the instruction is the slowable instruction, means for delaying processing of the instruction.

52. (New) The system of claim 51, wherein the means for delaying the processing of the instruction comprises means for delaying decoding of the instruction.